IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

#18
1BCB
9/30/02

Applicant:	Rodney Ruesch	Group Art Unit:	2819
Serial No.:	09/620,679	Examiner:	Don Le
Filed:	July 20, 2000	Docket:	499.075US1
Title:	GTL + DRIVER		

APPELLANT'S BRIEF ON APPEAL

Box AF
Commissioner for Patents
Washington, D.C. 20231

Sir:

This brief is presented in support of the Notice of Appeal filed on July 15, 2002 and received in the USPTO on July 22, 2002, from the final rejection of claims 7-16 and 23-25 of the above-identified patent application as set forth in the final Office Action dated March 14, 2002.

This brief is filed in triplicate and accompanied by the requisite fee set forth in 37 C.F.R. § 1.17(c). Please charge any additional fees or apply credits to deposit account number 19-0743.

Appellant respectfully requests reversal of the Examiner's rejection of claims 7-16 and 23-25 for various reasons, including those discussed below.

Table of Contents

Real Party in Interest

The real party in interest of the above-captioned patent application is the assignee, Silicon Graphics, Inc.

Related Appeals and Interferences

There are no related appeals or interferences known to the Appellant which will have a bearing on the Board's decision herein.

Status of the Claims

Claims 7-16 and 23-25 are pending, all of which have been rejected. Claims 1-22 were originally filed with the application. A restriction requirement identified three groups of claims and in a response to restriction requirement, a provisional election was made to prosecute the second group having claims 7-16. Claims 23-25 were added by amendment with the election and claims 1-6 and 17-22 were withdrawn.

In an Office Action dated October 10, 2001, claims 7-10, 15, 16 and 23-25 were rejected and claims 11-14 were objected to. In particular, claims 7 and 23-25 were rejected under 35 U.S.C. § 102(b) as being anticipated by Knee et al. (U.S. 5,337,254), hereinafter "Knee," and claims 8-10, 15 and 16 were rejected under 35 U.S.C. § 102(e) as being anticipated by Esch, Jr. (U.S. 6,118,310), hereinafter "Esch."

A response dated January 10, 2002 included traversals of the rejections.

An Office Action dated March 14, 2002 included final rejections of claims 7-10, 15, 16 and 23-25.

An after-final amendment and response dated May 13, 2002 included an amendment to claim 7.

An Advisory Action dated June 13, 2002 stated that the proposed amendment would not be entered because they raise new issues that would require further consideration and/or search.

A Notice of Appeal from the decision of the examiner was filed on July 15, 2002. The pending claims on appeal, numbered 7-16 and 23-25, are set forth in Appendix A.

Status of Amendments

Claims 7-16 were originally filed with the application and claims 23-25 were entered in an Amendment and Response dated July 19, 2001. A proposed amendment to claim 7, submitted in an Amendment and Response dated May 13, 2002, was denied entry. Following the denial of entry of the May 13, 2002 amendment, the claims remain as originally filed.

Summary of the Invention

Appellant's invention, as recited by independent claim 7, provides a method for communicating data in an integrated circuit using internal interconnects, one embodiment of which is disclosed on page 9, lines 5 *et seq.* relative to Fig. 2A. The method entails, *inter alia,* adjusting a first resistance coupled to a first supply voltage, adjusting a second resistance coupled to a second supply voltage and adjusting a third resistance coupled to the second supply voltage. The first, second and third resistances are programmably selectable based on a manufacturing process, supply voltage and temperature. The edge rate for logic level transitions, or other parameters, can be selected to provide efficient energy transfer between the driver and a receiver.

Edge rate compensation is disclosed in various portions of the specification, including page 3, lines 12 *et seq.* and page 12, lines 5 *et seq.* Edge rate compensation includes adjusting a binary predriver. In one embodiment, selecting an edge rate of a driver coupled to the divider network comprises executing programming for selecting resistance elements from a plurality of switchable resistance elements.

Issues

A. Whether claims 7 and 23-25 are anticipated under 35 U.S.C. § 102(b) by Knee et al. (U.S. 5,337,254).

B. Whether claims 8-10, 15 and 16 are anticipated under 35 U.S.C. § 102(e) by Esch, Jr. (U.S. 6,118,310).

Grouping of Claims

Appellant submits that the claims are to be treated in five groups as follows: claims 7 and 23-25; claims 8 and 10; claim 9; claim 15; and claim 16.

Argument

I. Rejections under 35 U.S.C. § 102(b)

Claims 7 and 23-25 were rejected under 35 U.S.C. §102(b) as being anticipated by Knee. Claims 8-10, 15 and 16 were rejected under 35 U.S.C. § 102(e) as being anticipated by Esch. Appellant respectfully traverses the rejection.

A. The Applicable Law

Anticipation requires that a single prior art reference must contain all the elements of the claim. *E.g., Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 231 U.S.P.Q. 81 (Fed. Cir. 1986). Anticipation exists only if all the elements of the claimed invention are present in a product or process disclosed, expressly or inherently, in a single prior art reference. *RCA Corp. v. Applied Digital Data Sys., Inc.*, 730 F.2d 1440, 221 U.S.P.Q. 385 (Fed. Cir. 1984), *cert. dismissed sub nom. Hazeltine Corp. v. RCA Corp.*, 468 U.S. 1228 (1984); *see also*, M.P.E.P. 706.02.

B. The Rejection of Claims 7 and 23-25 Under 35 U.S.C. § 102(b) Should Be Reversed

Appellant respectfully submits that claims 7 and 23-25 are not anticipated by Knee and respectfully traverses the rejection as follows.

In rejecting claim 7, the Office Action asserted:

> . . . that Knee teaches . . .
>
> adjusting a first resistance (activating transistor 1X connected to VDD at 110, figure 3) coupled to a first supply voltage (VDD), based on a manufacturing process, the first supply voltage and a temperature (PVT control signal from 18 through microprocessor to 70, figure 1);
>
> adjusting a second resistance (activating another transistor 1X connected to ground at 110, figure 3) coupled to a second supply voltage (ground), based on the manufacturing process, the first supply voltage and the temperature (PVT control signal from 18 through microprocessor to 70, figure 1);
>
> adjusting a third resistance (activating another transistor 2X connected to ground at 112, figure 1) coupled to a second supply voltage (ground), based on the manufacturing process, the first supply voltage and the temperature (PVT control signal from 18 through microprocessor to 72.

Appellant respectfully traverses the assertion and submits that *prima facie* anticipation has not been established because all elements recited in claim 7 are not taught by the cited document. For example, Appellant is unable to find a teaching of a second supply voltage in Knee. The May 14, 2002 Office Action asserted that:

> ". . . the claim does not specify the second supply voltage to be at a certain potential. Therefore, ground supply voltage is broadly interpreted as a second supply. Therefore, the claimed element is anticipated.

Appellant respectfully submits that "ground supply voltage" is oxymoronic and cannot properly be construed as "a second supply voltage," as recited in the claim. Ground provides a reference point by which the first supply voltage and the second supply voltage are measured. It appears inconsistent to refer to the ground as a supply voltage. Appellant finds no support for the Examiner's position of interpreting "ground" as "a second supply voltage," in the record. Appellant respectfully submits that the Examiner has not adequately described how the subject matter recited in claim 7 reads on Knee. Thus, the Examiner has not shown how Knee anticipates the subject matter recited in claim 7.

Appellant is unable to discern, from the Office Action, where Knee teaches or suggests that "ground" fulfills the claim element "second supply voltage." Appellant has requested that the Examiner provide a citation to an authority in support of that interpretation. Appellant's request was met with silence.

Appellant respectfully requests that the 35 U.S.C. § 102(b) rejection of claim 7, as well as claims 23-25, be reversed.

C. The Rejection of Claims 8 and 10 Under 35 U.S.C. § 102(e) Should Be Reversed

Appellant respectfully submits that claim 8 is not anticipated by Esch and respectfully traverses the rejection as follows.

In rejecting claim 8, the Office Action asserted:

> Esch teaches . . .
> selecting a resistance of a divider network (select resistor based on 262, 264 of figure 6) based on a manufacturing process, a supply voltage and a temperature;
> selecting an edge rate of a driver (edge rate is controlled by 266) coupled to the divider network, the selected edge rate based on the manufacturing process, the supply voltage and the temperature;
> receiving a data signal (203); and
> providing an output (output at 241) based on the data signal, the resistance, and the edge rate.

Appellant is unable to find support for the above assertions in Esch. For example, Appellant is unable to find a description of how a resistance is selected for resistors 262 and 264 based on a manufacturing process, a supply voltage and a temperature. In the portion of Esch cited in the Office Action, Appellant finds no teaching concerning a manufacturing process, a supply voltage or a temperature. In addition to the portion cited in the Office Action, resistors 262 and 264 are discussed at column 8, lines 49-55, however, even in this portion, Appellant is unable to find a teaching of selecting a resistance based on a manufacturing process, a supply voltage and a temperature.

In the Response to the Arguments section of the March 14, 2002 Office Action, the Examiner references column 5, lines 5-15. Appellant, however, respectfully submits that this

portion of Esch does not correlate a manufacturing process, a supply voltage or a temperature to the selection of resistors 262 and 264. Furthermore, Appellant respectfully notes that Figure 6, in which resistors 262 and 264 appear, is described as " . . . calibration circuitry. . ." (column 9, line 43). Thus, Appellant submits that Figure 6 does not teach a method of communicating data in an integrated circuit using internal interconnects, as recited in claim 8.

In addition, Appellant is unable to find, in Esch, a teaching of selecting an edge rate of a driver coupled to the divider network, the selected edge rate based on the manufacturing process, the supply voltage and the temperature. At page 4, the Office Action asserts that the edge rate is controlled by 266. At page 7, the Examiner states that although "Esch does not specifically written anywhere in the specification concerning edge rate. . . . This feature is inherent in the apparatus of Esch as shown in figure 4, by activating certain transistors (211..229), the edge rate of the driver depends on which transistors are activated." Instead, Esch is describing a method of adjusting output impedance to reflect changes in process, voltage and temperature. Although these selections may have some effect on edge rate, there is no step in Esch of "selecting an edge rate" as defined by Appellant and recited in claims 8-10, 15 and 16.

With reference to M.P.E.P. § 2112, the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. Here, it appears that the Office Action has not set forth support for the mere possibility of finding a teaching of "selecting an edge rate" in Esch. Thus, it follows, it is improper to conclude that, in fact, Esch actually teaches "selecting an edge rate."

Appellant respectfully requests that the 35 U.S.C. § 102(e) rejection of claims 8 and 10 be reversed.

D. The Rejection of Claims 9, 15 and 16 Under 35 U.S.C. § 102(e) Should Be Reversed

Appellant hereby incorporates the arguments presented above for claim 8 in support of patentability for claims 9, 10, 15 and 16. Appellant respectfully submits that the arguments presented in claim 8 are sufficient to overcome the rejection of claims 9, 10, 15 and 16 under 35 U.S.C. § 102(e) and properly distinguishes the present invention over Esch. Furthermore, Appellant respectfully submits claims 9, 10, 15 and 16 are patentable as further limitations of patentable base claim 8.

As for claim 9, the Examiner stated that Esch does not show "'word for word' of maintaining a substantially constant edge rates as claimed by applicant [sic]." However, pursuant to M.P.E.P. § 2131, for *prima facie* anticipation, "the identical invention must be shown in as complete detail as is contained in the ... claim." Appellant was left with the impression that the Examiner was relying on some form of official notice. An earlier request for a citation to an authority in support of the assertion was ignored.

As for claim 15, the Examiner stated that "Figure 5 of Esch shows an enable signal (ENABLE) controlling a switchable resistance element 230." Appellant traverses the assertion that this anticipates receiving a tristate enable signal; and actuating a switchable resistance element in response to the tristate enable signal, as recited in claim 15. At column 7, line 23 of Esch discussing element 230, as well as at the cited figure, Appellant is unable to find a teaching, for example, of receiving a tristate enable signal.

As for claim 16, the Examiner stated that "Figure 5 of Esch shows the output of the switching element 230 is an inverted output based on the enable signal." Appellant, on the other, unable to find, in Esch, a teaching of a programmable inverter, as recited in claim 16.

Appellant respectfully requests that the 35 U.S.C. § 102(e) rejection of claims 9, 15 and 16 be reversed.

Allowed Claims

The Office Action notes objections to claims 11-14. Appellant respectfully submits that the base claims are in condition for allowance as presented above. Consequently, Appellant respectfully submits that claims 11-14 are in condition for allowance.

Appellant respectfully requests allowance of claims 11-14.

Conclusion

For the foregoing reasons, it is submitted that the rejection of claims 7-16 and 23-25 is improper. Reversal is respectfully requested. Should the Board be of the opinion that a rejected claim may be allowable in amended form, an explicit statement to that effect is also respectfully requested.

Respectfully submitted,

RODNEY RUESCH
By their Representatives,
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6911

Date September 19, 2002 By _____
David W. Black
Reg. No. 42,331

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: BOX AF, Commissioner of Patents, Washington, D.C. 20231, on this 19 day of Sept., 2002.

Candis B. Buending
Name

_____
Signature

APPENDIX A
The Claims on Appeal

GTL + DRIVER
Applicant: Rodney Ruesch
Serial No.: 09/620,679

7. A method of communicating data in an integrated circuit using internal interconnects, the method comprising:

receiving a data signal;

adjusting a first resistance coupled to a first supply voltage, based on a manufacturing process, the first supply voltage and a temperature;

adjusting a second resistance coupled to a second supply voltage, based on the manufacturing process, the first supply voltage and the temperature; and

adjusting a third resistance coupled to the second supply voltage, based on the manufacturing process, the first supply voltage and the temperature.

8. A method of communicating data in an integrated circuit using internal interconnects, the method comprising:

selecting a resistance of a divider network based on a manufacturing process, a supply voltage and a temperature;

selecting an edge rate of a driver coupled to the divider network, the selected edge rate based on the manufacturing process, the supply voltage and the temperature;

receiving a data signal; and

providing an output based on the data signal, the resistance, and the edge rate.

9. The method of claim 8 wherein selecting an edge rate of a driver coupled to the divider network comprises maintaining a substantially constant edge rate.

10. The method of claim 8 wherein providing an output comprises turning on a PFET transistor and turning off an NFET transistor.

11. The method of claim 8 wherein selecting a resistance of a divider network comprises selecting a plurality of parallel resistance elements.

12. The method of claim 8 wherein selecting a resistance of a divider network comprises executing programming for selecting resistance elements from a plurality of switchable resistance elements.

13. The method of claim 8 wherein selecting an edge rate of a driver coupled to the divider network comprises selecting a plurality of parallel resistance elements.

14. The method of claim 8 wherein selecting an edge rate of a driver coupled to the divider network comprises executing programming for selecting resistance elements from a plurality of switchable resistance elements.

15. The method of claim 8 further comprising:
receiving a tristate enable signal; and
actuating a switchable resistance element in response to the tristate enable signal.

16. The method of claim 15 wherein actuating a switchable resistance element comprises actuating a programmable inverter.

23. The method of claim 7 wherein adjusting a first resistance includes changing a resistance of a semiconductor.

24. The method of claim 7 wherein adjusting a first resistance includes changing a gate voltage on a field effect transistor (FET).

25. The method of claim 7 wherein adjusting a first resistance includes selecting a predetermined number of programmable bits from a plurality of programmable bits.